

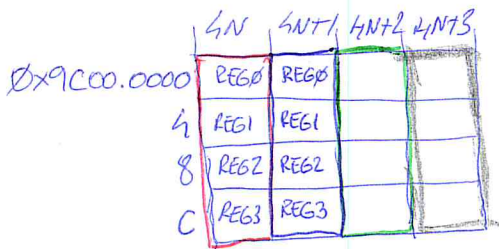
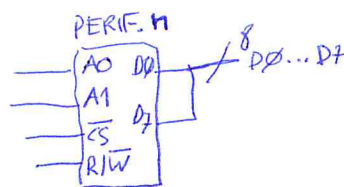
TEMA 5 (EJERCICIOS)

EJERCICIO 1

4 PERIFÉRICOS 8bits (4 REGISTROS)

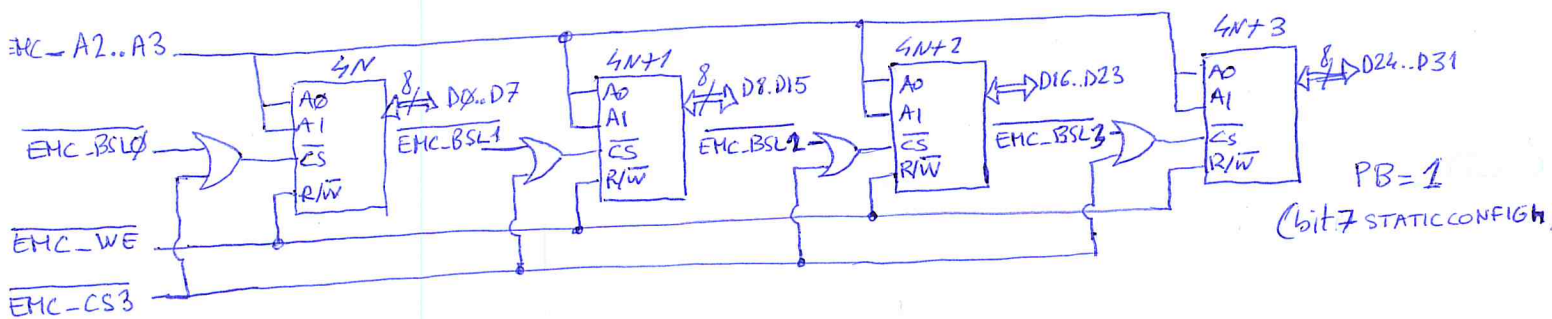
$0x9C00.0000 \rightarrow EMC-CS3$

Modo 32 bits (MW=00) \rightarrow 4 BANCOS



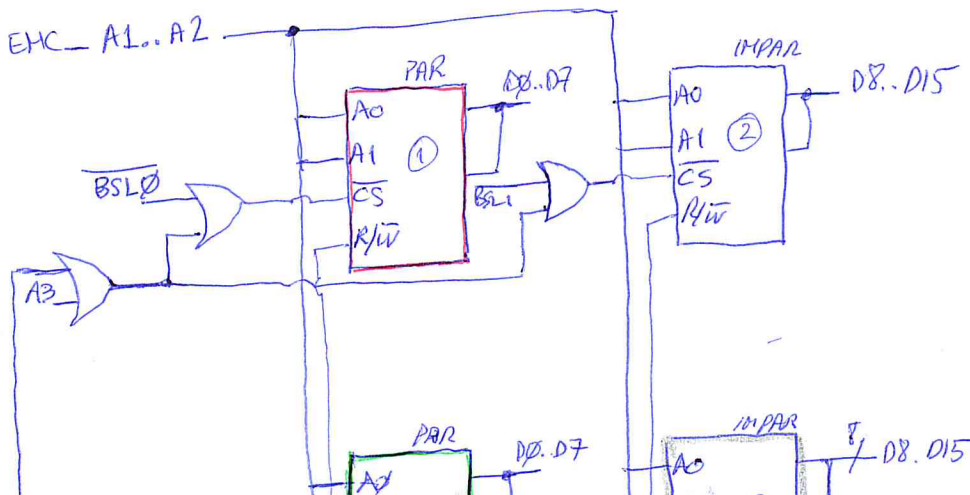
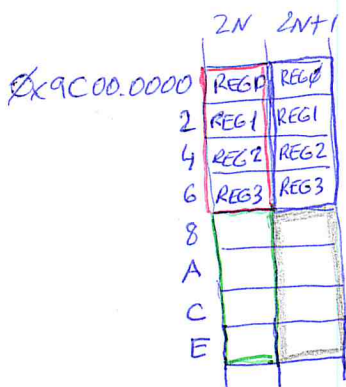
- PERIF. 1
- PERIF. 2
- PERIF. 3
- PERIF. 4

LITTLE-ENDIAN (Reset) !



Modo 16 bits (MW=01) 2 BANCOS

LITTLE-ENDIAN (Reset)



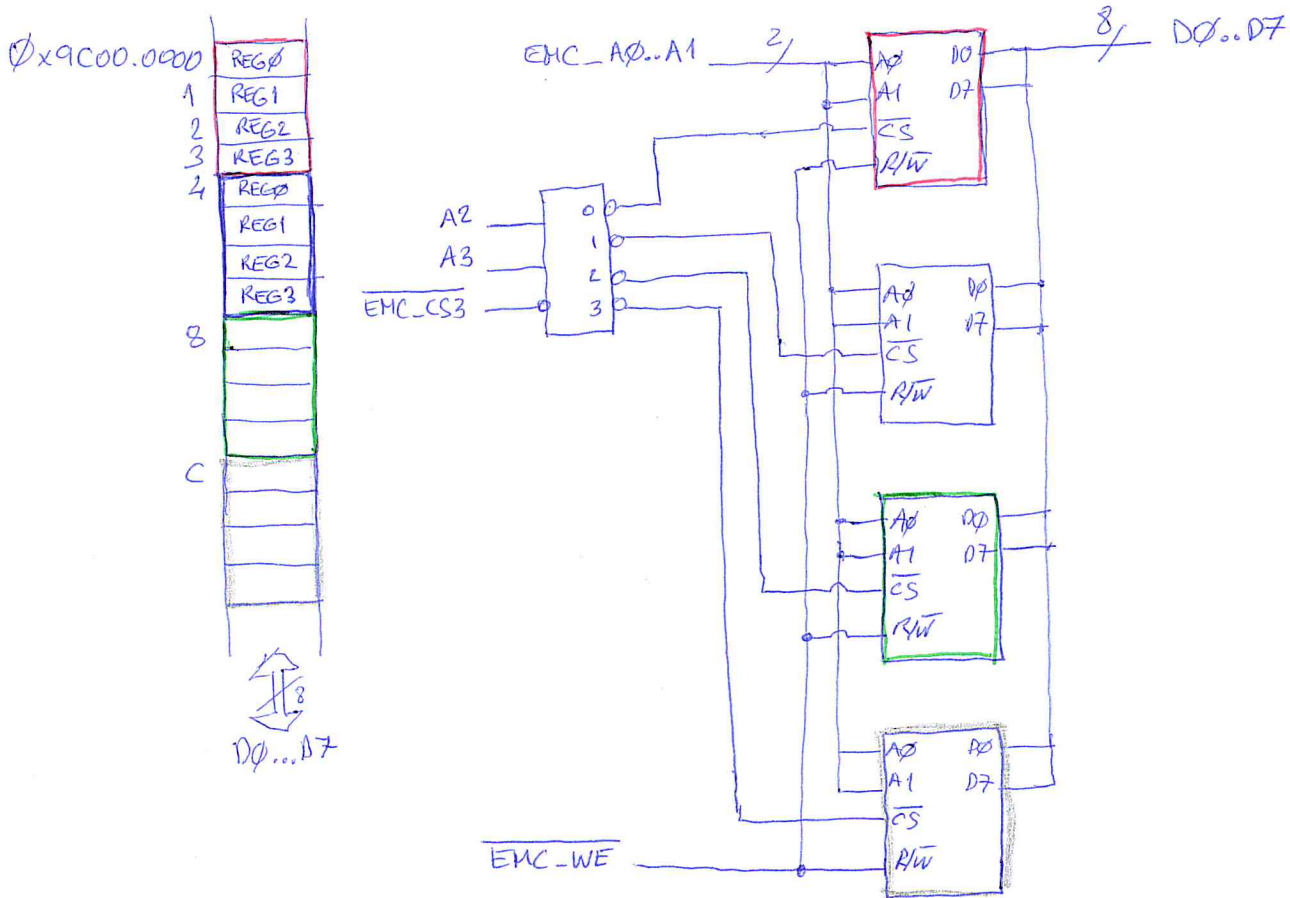
CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
LLAMA O ENVÍA WHATSAPP: 689 45 44 70

ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
CALL OR WHATSAPP: 689 45 44 70



EJERCICIO 1 (Continuación)

MOD0 8 bits (MW=00) reset



Ojo! No intervienen las líneas de selección de bancos (EMC_BLSn)

Cartagena99

CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
LLAMA O ENVÍA WHATSAPP: 689 45 44 70

ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
CALL OR WHATSAPP:689 45 44 70

EJERCICIO 2

ROM — 1Mbyte (4 x 256Kx8)

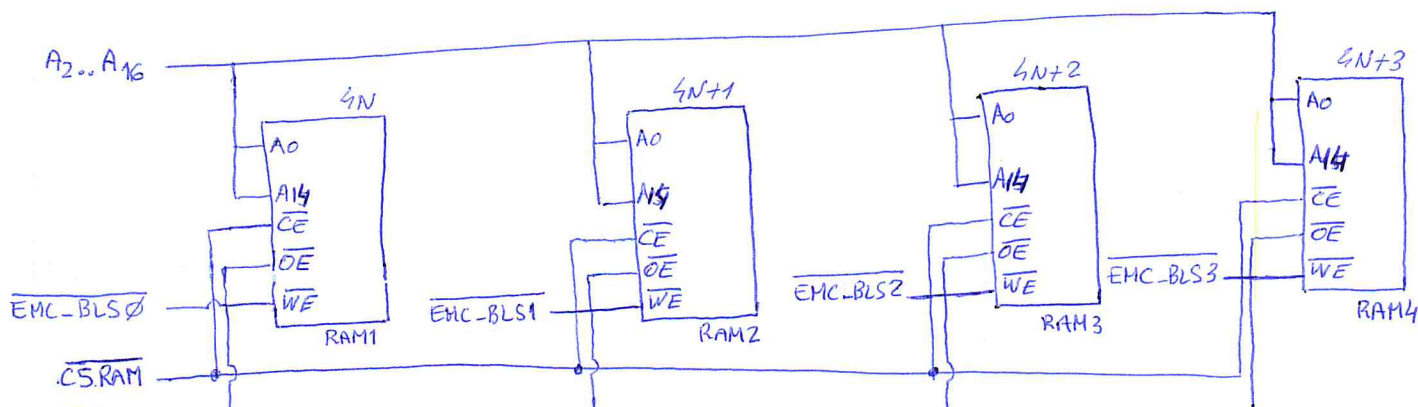
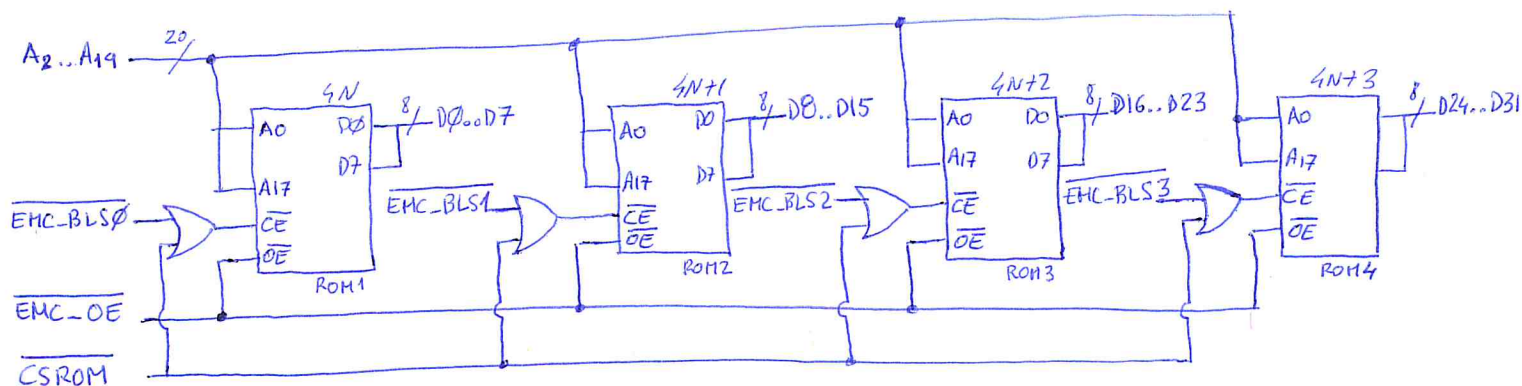
RAM — 128Kbytes (4 x 32Kx8)

MEMO 32bits (4 bancos)

DIRECCIONES	
0x8000.0000	ROM (1Mbyte)
0x800F.FFFF	
0x8010.0000	RAM (128Kbytes)
0x8011.FFFF	

$$\overline{CS}_{ROM} = A_{20} + \overline{EMC_CS\phi}$$

$$\overline{CS}_{RAM} = A_{20} + A_{19} + A_{18} + A_{17} + \overline{EMC_CS\phi}$$



CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
LLAMA O ENVÍA WHATSAPP: 689 45 44 70

ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
CALL OR WHATSAPP: 689 45 44 70

Cartagena99

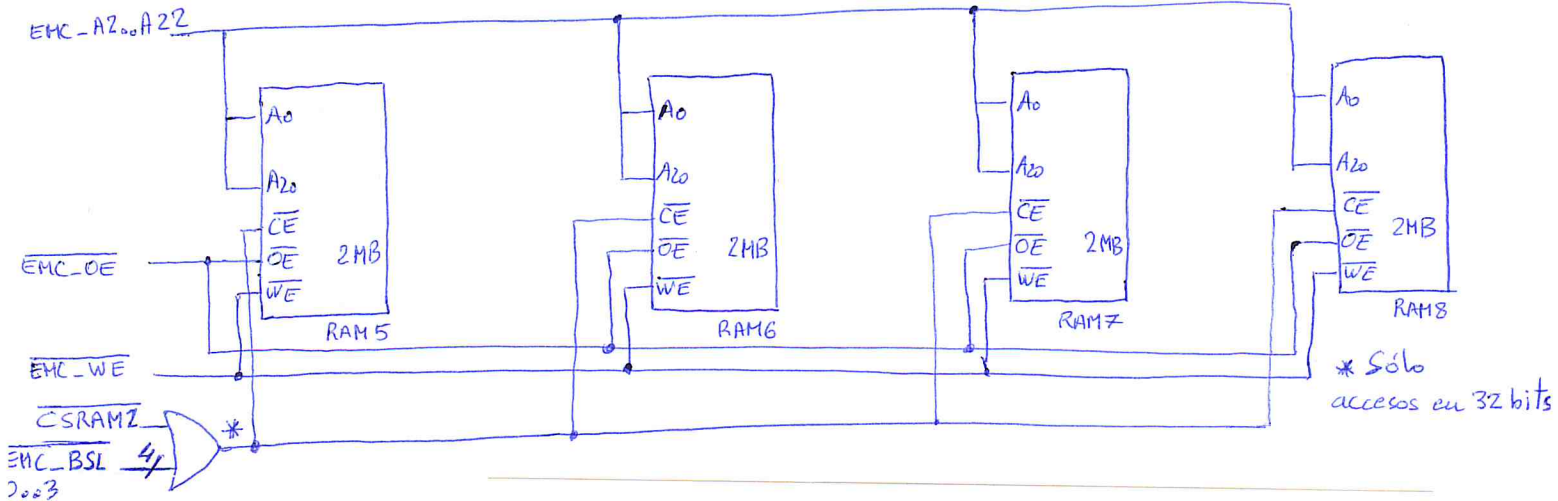
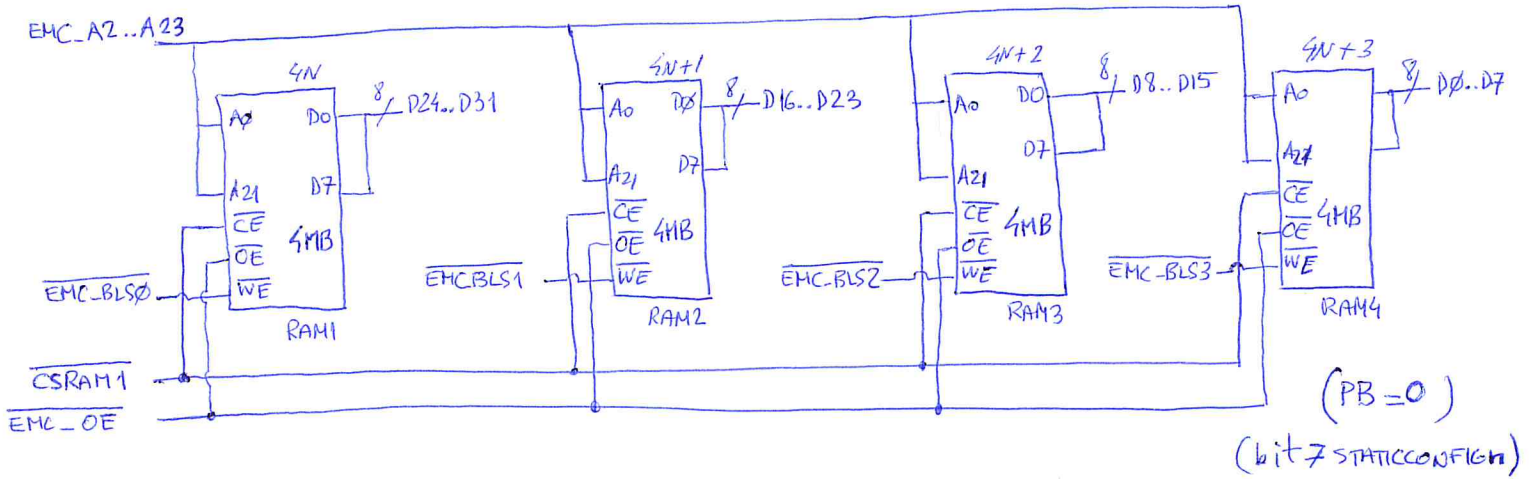
EJERCICIO 3

LPC1788 → BIG ENDIAN!
Dispositivos de 8 bits

o Caso 2

- 16 MB de SRAM con accesos en tamaño 8, 16 y 32 bits.
- 8 MB " " " " " " " 32 bits.
- 256KB periféricos " " " " " " " 8 bits.

EMC-CS0 → 0x9000.0000 → SRAM → Ancho de bus 32 bits → STATCONFIG1 (HW=0)
EMC-CS0 → 0x8000.0000 → PERIF. → " " " 8 bits → STATCONFIG0 (HW=0)

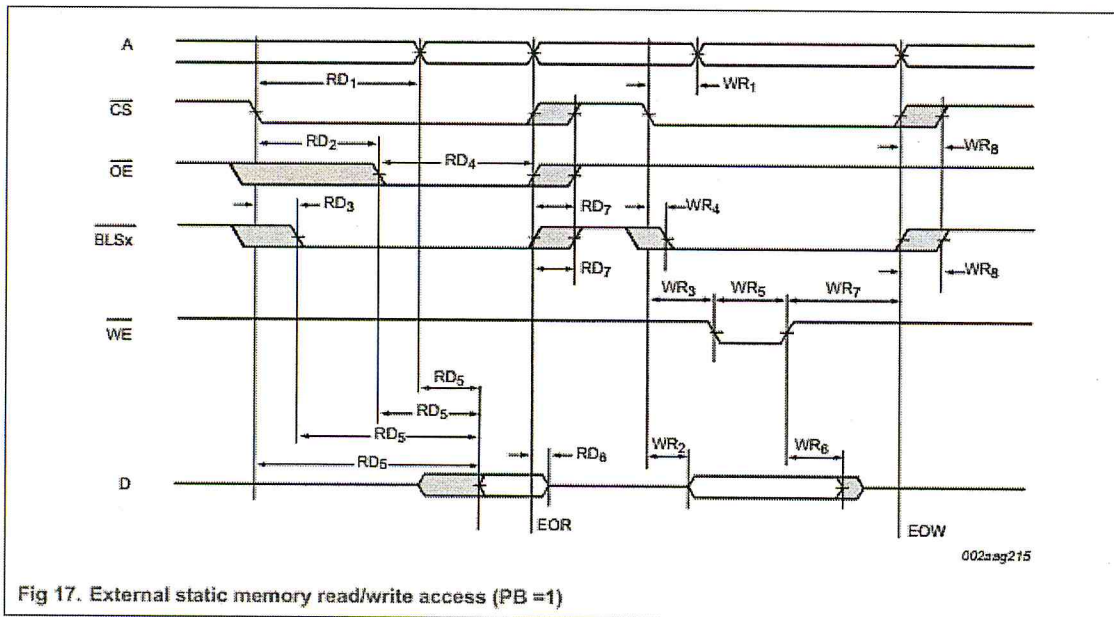
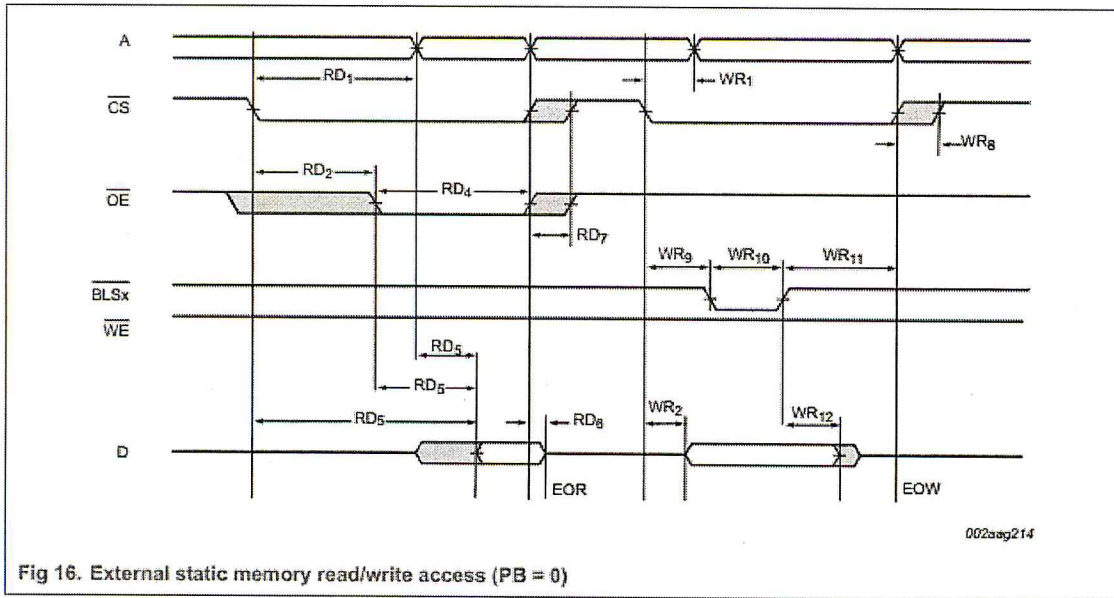


DIRECCIONES

CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
LLAMA O ENVÍA WHATSAPP: 689 45 44 70

ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
CALL OR WHATSAPP:689 45 44 70





**CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
 LLAMA O ENVÍA WHATSAPP: 689 45 44 70**

- - -

**ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
 CALL OR WHATSAPP:689 45 44 70**

Table 134. Static Memory Configuration registers (STATICCONFIG[0:3], address 0x2009 C200 (STATICCONFIG0), 0x2009 C220 (STATICCONFIG1), 0x2009 C240 (STATICCONFIG2), 0x2009 C260 (STATICCONFIG3)) bit description

Bit	Symbol	Value	Description	Reset Value
1:0	MW		Memory width.	0
		0x0	8 bit (POR reset value).	
		0x1	16 bit.	
		0x2	32 bit.	
		0x3	Reserved.	
2	-		Reserved. Read value is undefined, only zero should be written.	NA
3	PM		Page mode. In page mode the EMC can burst up to four external accesses. Therefore devices with asynchronous page mode burst four or higher devices are supported. Asynchronous page mode burst two devices are not supported and must be accessed normally.	0
		0	Disabled (POR reset value).	
		1	Asynchronous page mode enabled (page length four).	
5:4	-		Reserved. Read value is undefined, only zero should be written.	NA
6	PC		Chip select polarity. The value of the chip select polarity on power-on reset is 0.	0
		0	Active LOW chip select.	
		1	Active HIGH chip select.	
7	PB		Byte lane state. The byte lane state bit, PB, enables different types of memory to be connected. For byte-wide static memories the $\overline{BLS3:0}$ signal from the EMC is usually connected to \overline{WE} (write enable). In this case for reads all the $\overline{BLS3:0}$ bits must be HIGH. This means that the byte lane state (PB) bit must be LOW. 16 bit wide static memory devices usually have the $\overline{BLS3:0}$ signals connected to the \overline{UBn} and \overline{LBn} (upper byte and lower byte) signals in the static memory. In this case a write to a particular byte must assert the appropriate \overline{UBn} or \overline{LBn} signal LOW. For reads, all the \overline{UB} and \overline{LB} signals must be asserted LOW so that the bus is driven. In this case the byte lane state (PB) bit must be HIGH.	0
		0	For reads all the bits in $\overline{BLS3:0}$ are HIGH. For writes the respective active bits in $\overline{BLS3:0}$ are LOW (POR reset value).	
		1	For reads the respective active bits in $\overline{BLS3:0}$ are LOW. For writes the respective active bits in $\overline{BLS3:0}$ are LOW.	

Cartagena99

CLASES PARTICULARES, TUTORÍAS TÉCNICAS ONLINE
LLAMA O ENVÍA WHATSAPP: 689 45 44 70

ONLINE PRIVATE LESSONS FOR SCIENCE STUDENTS
CALL OR WHATSAPP:689 45 44 70